REMARKS

The Office Action of June 9, 2008 has been received and its contents carefully considered.

The present Amendment corrects claim 21 in response to the objection in section 5 of the Office Action. Accordingly, it is respectfully submitted that the objection has been overcome.

Section 2 of the Office Action objects to the drawings on the ground that Figure 3(c) shows no indication that the polysilicon arrangement is etched, and section 4 objects to changes in the specification regarding Figure 3(c). Section 4 comments, "Specifically, there is nothing in the original disclosure which supports there being a structure remaining in the non-doped polysilicon region after the described etching process." For the reasons discussed below, the objections in both sections 2 and 4 of the Office Action are respectfully traversed.

The present application discloses that P-type polysilicon and N-type polysilicon etch at different rates (see, for example, the paragraph bridging pages 2 and 3 of the application and the paragraph bridging pages 7 and 8). The application also discloses that non-doped polysilicon etches at a rate which lies between the etching rate of P-type polysilicon and N-type polysilicon (see the paragraph at page 7 of the application, lines 14-25). Since both a P-type polysilicon gate electrode and an N-type polysilicon gate electrode are shown in the original version of Figure 3(c), what the application calls a "dummy gate" of non-doped polysilicon should be present in Figure 3(c).

Furthermore, Figure 3(a) shows implantation of N-type impurities into a region 4 through an opening in resist 3. Figure 3(b) shows implantation of P-type impurities in a region 5 through an opening in a resist layer; the region 6 is not implanted with impurities. The drawings do not show a mask with patterns for etching the N-type and P-type gate electrodes that are shown in Figure 3(c), but an ordinarily skilled person would have understood that a mask is used to permit etching of these gate electrodes. The application advises that dummy gate patterns are disposed on the mask (see page 7, lines 3-7). An ordinarily skilled person would have realized that the result would be a dummy gate electrode in Figure 3(c) as in the replacement drawing sheet that was forwarded with the last Amendment.

Section 6 of the Office Action rejects claims 20 and 21 for failing to comply with the written description requirement of 35 USC 112, first paragraph. The rejection is respectfully traversed.

The rejected claims provide that the non-doped polysilicon arrangement is electrically disconnected from all of the transistors on the semiconductor device. The fact that the application calls a non-doped polysilicon arrangement a "dummy gate" clearly implies that it is not part of the working circuitry and is therefore isolated from the transistors that are present in the working circuitry. An ordinarily skilled person would have realized that the dummy gate is fabricated not for use in a circuit but as an aid to etching the gate electrodes of transistors that are part of the working circuitry. It is therefore respectfully submitted that an ordinarily skilled person who had read the application would have realized that the inventor was in mental possession on a non-doped polysilicon arrangement that is electrically disconnected from the transistors.

Section 7 of the Office Action rejects independent claim 15 (along with several dependent claims) for obviousness based on US patent 5,783,850 to Liau et al in view of US patent 6,541,359 to Gabriel et al (these references will hereafter be called simply "Liau" and "Gabriel" for the sake of convenient discussion), with evidence provided by US patent 4,989,057 to Lu. The rejection is respectfully traversed.

Independent claim 15 provides that a non-doped polysilicon arrangement occupies an area "that is larger than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode." The Office Action asserts that Lu teaches that the gate width a transistor is proportional to its current-carrying capacity, so the gate width is considered to be a result-effective variable. However, claim 15 refers to area, which is a function not only of width but also of length. Even if an ordinarily skilled person modified the length of Liau's non-doped gate electrode 40, in an attempt to achieve some desired current-carrying capacity for Liau's ESD transistor, there is no reason to suspect that the result would be a gate occupying an area that is larger than the total area occupied by the two gates 41 shown in Liau's Figure 7.

It is also respectfully submitted that an ordinarily skilled person who wanted to improve Liau's arrangement in some way would not have thought it necessary to optimize the current-carrying capacity of Liau's ESD protection transistor. The ordinarily skilled person would know that the purpose of an ESD protection transistor is

to protect circuitry from high voltage during a momentary voltage spike. The ordinarily skilled person would not expect an ESD event to last long enough that the current through an ESD protection transistor would cause appreciable heating. As a result, an ordinarily skilled person would not perceive a need to optimize the current-carrying capacitor of Liau's ESD protection transistor so as to depart from what Liau teaches and achieve a protection transistor with a non-doped polysilicon arrangement having an area larger than the area occupied by Liau's two gate electrodes 41.

Claim 15 also recites that "the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon arrangement." Even if an ordinarily skilled person did modify the gate width of Liau's non-doped gate electrode 40 in order to optimize the current-carrying capacity of Liau's ESD protection transistor (despite the above argument to the contrary), and even if this optimization resulted in a non-doped polysilicon arrangement "occupying an area that is larger than a total area occupied by the N type polysilicon gate electrode and a P type polysilicon gate electrode" as recited in claim 15, it is unlikely that the ordinarily skilled person would have perceived some link between optimization of current-carrying capacity and end-point detection during etching.

In view of these considerations, it is respectfully submitted that the rejection of independent claim 15 should be withdrawn.

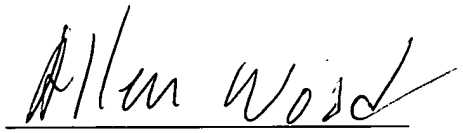
Section 8 of the Office Action rejects independent claim 3 (and also various dependent claims) for anticipation by Liau, Gabriel, and US patent 5,665,203 to Lee et al (with evidence provided by Lu).

Like claim 15, claim 3 recites that a non-doped polysilicon arrangement occupies "an area that is larger than a total area occupied by the N type polysilicon gate electrode and the P type polysilicon gate electrode." Similar to claim 15, claim 3 recites that "an end point detection of one of the stages of the etching process is based on the etching of the non-doped polysilicon arrangement." For the reasons discussed above with respect to claim 15, it is respectfully submitted that Liau, Gabriel, and Lu would not have provided an incentive for an ordinarily skilled person to achieve the method defined by claim 3. The Lee et al reference does not remedy the deficiencies of Liau, Gabriel, and Lu, so the rejection of claim 3 should also be withdrawn.

The remaining claims depend from the independent claims discussed above and recite additional limitations to further define the invention. They are therefore automatically patentable along with their independent claims and need not be further discussed. It is nevertheless noted that dependent claims 20 and 21 provide that "the non-doped polysilicon arrangement is electrically disconnected from all of the transistors in the semiconductor device," which is inconsistent with the non-doped gate electrode 40 in Liau's ESD protection transistor. An ordinarily skilled person who wanted to improve Liau's arrangement in some way would not disconnect Liau's ESD protection transistor.

For the foregoing reasons, it is therefore respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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